



APPENDIX D

**(VERSION OF CLAIMS AS AMENDED HEREIN
WITH MARKINGS TO SHOW CHANGES MADE)**

(Serial No. Not yet assigned)



VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for producing [non-warped]nonwarped semiconductor die from a wafer having a [frontside]front side, a [backside]back side, and a [frontside]front side layer on a portion of said [semiconductor] wafer causing a stress, said method comprising:
reducing a cross-section of said semiconductor die by thinning [the]said semiconductor die;
applying a stress-balancing layer to said; and
singulating said wafer into a plurality of semiconductor die.
2. (Amended) A method in accordance with claim 1, wherein said [frontside]front side layer comprises a layer applied in fabrication of said semiconductor die.
3. (Amended) A method in accordance with claim 1, wherein said [frontside]front side layer comprises a layer of passivation material.
7. (Amended) A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer substantially covering said [backside]back side.
9. (Amended) A method in accordance with claim 1, wherein said stress-balancing layer comprises a plurality of portions, each said portion covering a selected portion of [the]said thinned semiconductor die on said wafer.
23. (Amended) A method in accordance with claim 1, wherein said semiconductor die comprises one of a DIP, SIP, ZIP, PLCC, SOJ, SIMM, DIMM, LOC, QFP, SOP, TSOP, and a flip-chip.
27. (Amended) A method in accordance with claim [23]25, further comprising exposing a portion of said material markable[material] with optical energy exposing at least a portion of

said material markable[material] to one of a Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser) or carbon dioxide laser.

28. (Amended) A method in accordance with claim 1, further comprising:
applying a tape over said stress-balancing layer, said tape comprising a UV-penetrable polyvinyl chloride tape having an acrylic UV-sensitive adhesive disposed thereon; and
~~ex~~posing a portion of said tape with optical energy exposing at least a portion of said tape to one of a Nd:YAG, Nd-YLP[,] or carbon dioxide laser.

29. (Amended) A method in accordance with claim 1, wherein said stress-balancing layer comprises a first [sub-layer]sublayer having high rigidity in the X-direction[,] and a second sub-layer having high rigidity in the Y-direction.

30. (Amended) A method in accordance with claim 1, wherein said stress-balancing layer comprises a layer having a coefficient of thermal expansion substantially similar to [the]a coefficient of thermal expansion of said [frontside]front side layer.

31. (Amended) A method in accordance with claim 1, further comprising applying a die-attach adhesive to at least a portion of [the]a surface of said stress-balancing layer.

32. (Amended) A method in accordance with claim 1, further comprising applying a temporary reinforcement layer over at least a portion of said [frontside]front side layer prior to thinning said [backside]back side.

33. (Amended) A method for producing a small Z-dimension [non-warped]nonwarped semiconductor die from a semiconductor wafer having a [frontside]front side, a [backside]back side, and a stress applied thereto by a [frontside]front side layer, said method comprising:
reducing a cross-section of said semiconductor die by thinning [the]said [backside]back side thereof;

applying a rigid stress-balancing layer to a portion of said thinned [backside]back side; and singulating said wafer into a plurality of [non-warped]nonwarped semiconductor dice.

34. (Amended) A method in accordance with claim 33, wherein said [frontside]front side layer comprises a layer applied in a microcircuit fabrication step.

35. (Amended) A method in accordance with claim 33, wherein said [frontside]front side layer comprises a layer of passivation material.

39. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer substantially covering said thinned [backside]back side.

41. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a plurality of discrete portions, each said portion covering a selected portion of the thinned [backside]back side of a die on said wafer.

42. (Amended) A method in accordance with claim 41, wherein said selected portion comprises a majority of said thinned die [backside]back side.

44. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned [backside]back side by one of a chemical vapor deposition (CVD) process, an evaporation process, and an epitaxy process.

45. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned [backside]back side by one of LPCVD, APCVD, MOCVD, PECVD, and UHVCVD.

46. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer applied to said thinned [~~backside~~]back side by one of VPE, MBE, and CMOSE.

59. (Amended) A method in accordance with claim 56, further comprising exposing a portion of said material markable[material] with optical energy exposing at least a portion of said material markable[material] to one of a Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser) or carbon dioxide laser.

60. (Amended) A method in accordance with claim [1]33, further comprising applying a tape over said stress-balancing layer, said tape comprising a UV-penetrable polyvinyl chloride tape having an acrylic UV-sensitive adhesive disposed thereon, and exposing a portion of said tape with optical energy exposing at least a portion of said tape to one of a Nd:YAG, Nd-YLP, or carbon dioxide laser.

61. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a first [sub-layer]sublayer having high rigidity in the X-direction, and a second [sub-layer]sublayer having high rigidity in the Y-direction.

62. (Amended) A method in accordance with claim 33, wherein said stress-balancing layer comprises a layer having a coefficient of thermal expansion substantially similar to that of said [~~frontside~~]front side layer.

63. (Amended) A method in accordance with claim 33, further comprising applying a die-attach adhesive to at least a portion of [~~the~~]an outer surface of said stress-balancing layer.

64. (Amended) A method in accordance with claim 33, further comprising applying a temporary reinforcement layer over said [~~frontside~~]front side layer prior to thinning said [~~backside~~]back side.

65. (Amended) A method for producing low Z-dimension [non-warped]nonwarped semiconductor dice having a die [frontside]front side, a die [backside]back side, and a stress applied thereto by a die [frontside]front side layer, said method comprising:
forming a semiconductor wafer having a [frontside]front side, a [backside]back side, a plurality of microcircuits on said [frontside]front side, and a [frontside]front side layer applying stress to said wafer;
reducing a cross-section of said semiconductor wafer by thinning [the]said [backside]back side thereof;
singulating said wafer into a plurality of semiconductor dice; and
applying a rigid stress-balancing layer to said thinned [backside]back side under conditions which apply a [backside]back side stress generally equivalent to said [front-side]front side stress upon restoration to conditions of said semiconductor die use.

66. (Amended) A method in accordance with claim 65, wherein said [frontside]front side layer comprises a layer of passivation material.

67. (Amended) A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said [backside]back side by one of a chemical vapor deposition (CVD) process, an evaporation process, and an epitaxy process.

68. (Amended) A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said [backside]back side by one of LPCVD, APCVD, MOCVD, PECVD, and UHVCVD.

69. (Amended) A method in accordance with claim 65, wherein said stress-balancing layer comprises a layer applied to said [backside]back side by one of VPE, MBE, and CMOSE.

75. (Amended) A semiconductor die, comprising:

a semiconductor substrate having a [frontside]front side and a [backside]back side;
an integrated circuit on a portion of said [frontside]front side;
a passivation layer covering a portion of said integrated circuit; and
a stress-balancing layer covering at least a portion of said [backside]back side.

80. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 79, wherein said adhesive layer comprises a layer of material for laser-marking.

81. (Amended) A [non-warp]nonwarp semiconductor die, comprising:
a semiconductor substrate having a [frontside]front side, a [backside]back side, and a low ratio of height to
a horizontal dimension;
an integrated circuit on said [frontside]front side;
a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate [frontside]front side;
a stress-balancing layer covering at least a portion of said [backside]back side, said stress-balancing layer for balancing a portion of said [frontside]front side stress with a generally equivalent [backside]back side stress.

82. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 81, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

83. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 81, wherein said stress-balancing layer comprises an adhesive material.

84. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 83, wherein said stress-balancing layer comprises a layer of material for laser-marking.

85. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 81, further comprising an adhesive layer attached to said stress-balancing layer.

86. (Amended) A [non-warp]nonwarp semiconductor die in accordance with claim 85, wherein said adhesive layer for laser-marking.